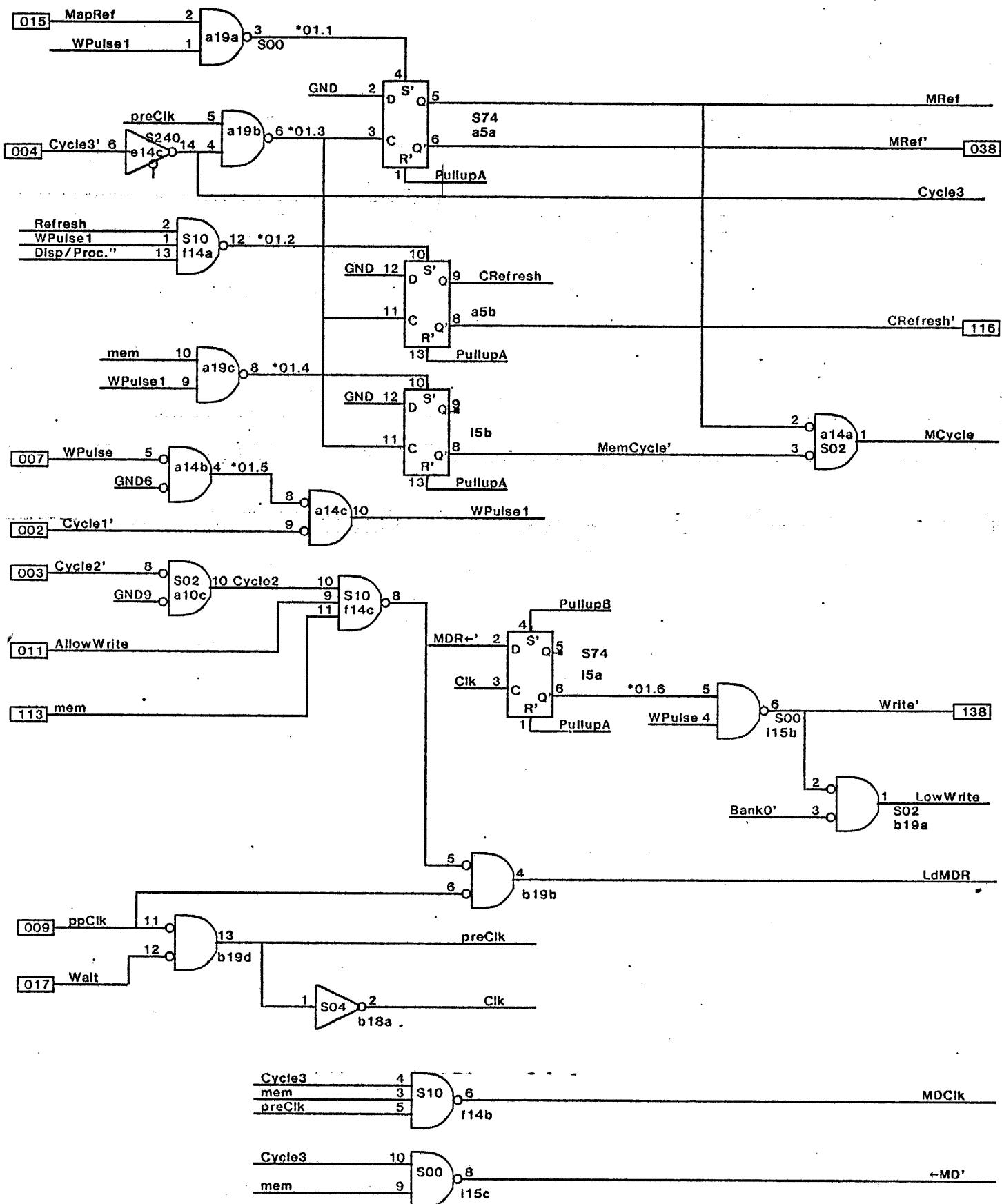


## Memory Control Card

1. Write, CRefresh', MRef, LdMDR, Cycle Rcv., MDClk, ←MD'
2. Refresh Counter & Cas Registers
3. Address Selection Logic, RASDIy, & LRASDIy
4. Memory Bank Selection
5. Drivers for Address, CAS', & Write'
6. Low Bank A
7. Low Bank B
8. Low Bank C
9. Low Bank D
10. Mem. Data Register, Mem. Control Reg., Check bit Gen.
11. Memory Chip data paths
12. Memory Data Buffers
13. Syndrome Generator
14. Error Correction Data paths
15. Error Log Register
16. Resistors and R-Dips
17. Caps Diodes and Fuses
18. Test Points
19. Material List
20. Board Layout

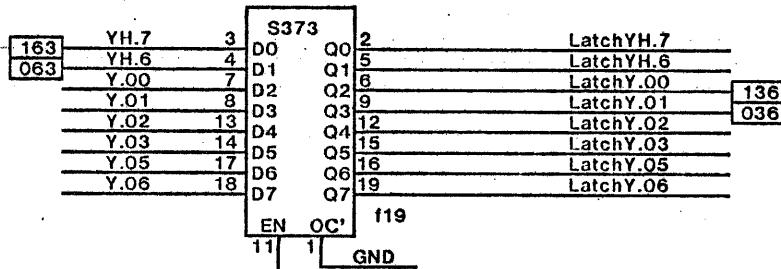
XEROX SDD	Project WS	REFERENCE Memory Control Card Dwg	File EMCTL00.sil	Designer Crane	Rev D	Date 3/19/80	Page 00
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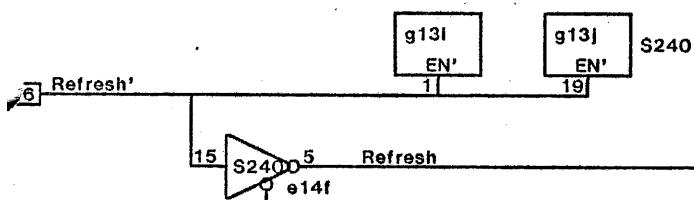
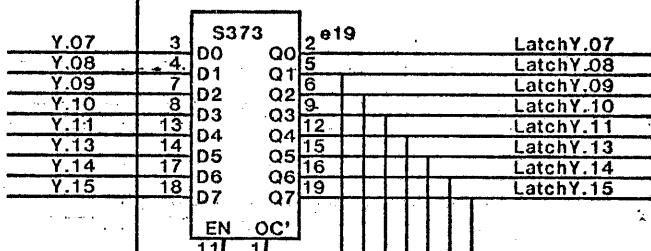
XEROX SDD	Project WS	Write, CRefresh', MRef, LdMDR, CycleRcv, MDClk, ←MD'	File EMCTL01.sil	Designer Crane	Rev D	Date 3/19/80	Page 1
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061	YH.2
161	YH.3
062	YH.4
162	YH.5

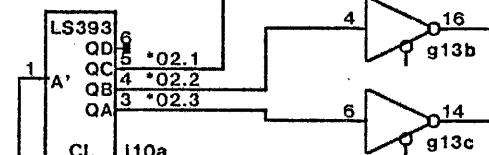
CAS Register



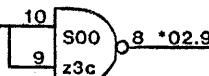
CasLatch



Refresh Counter

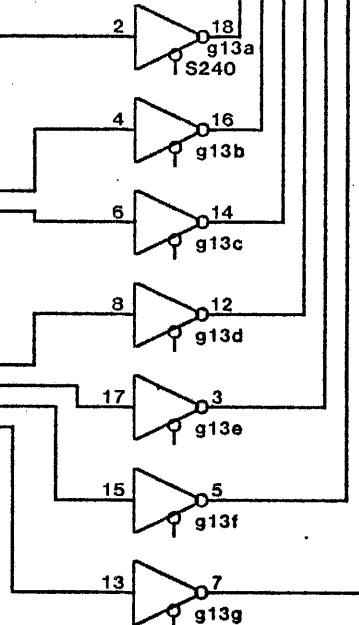
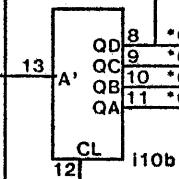
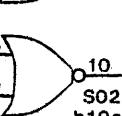


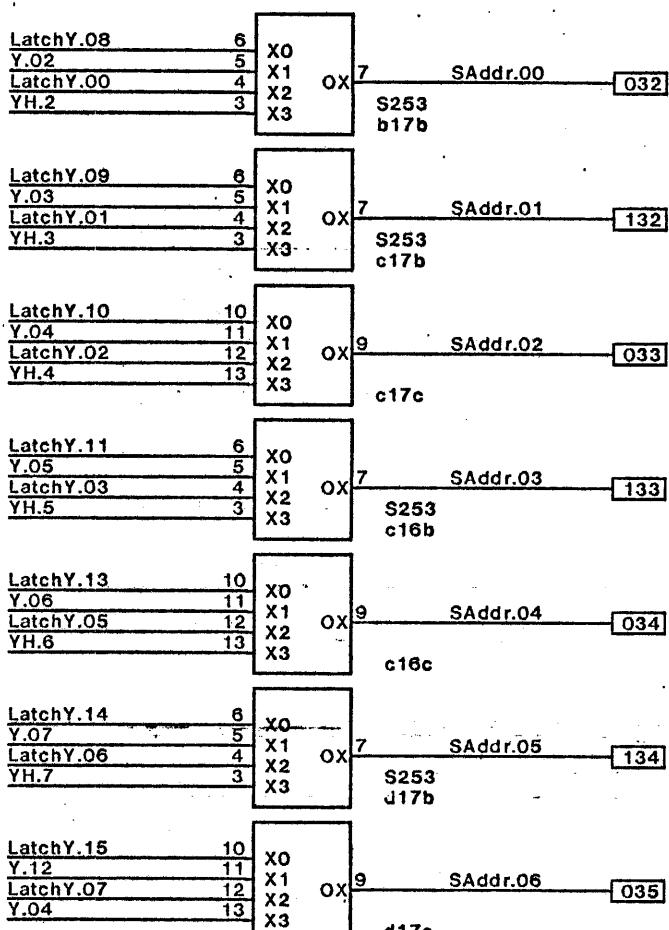
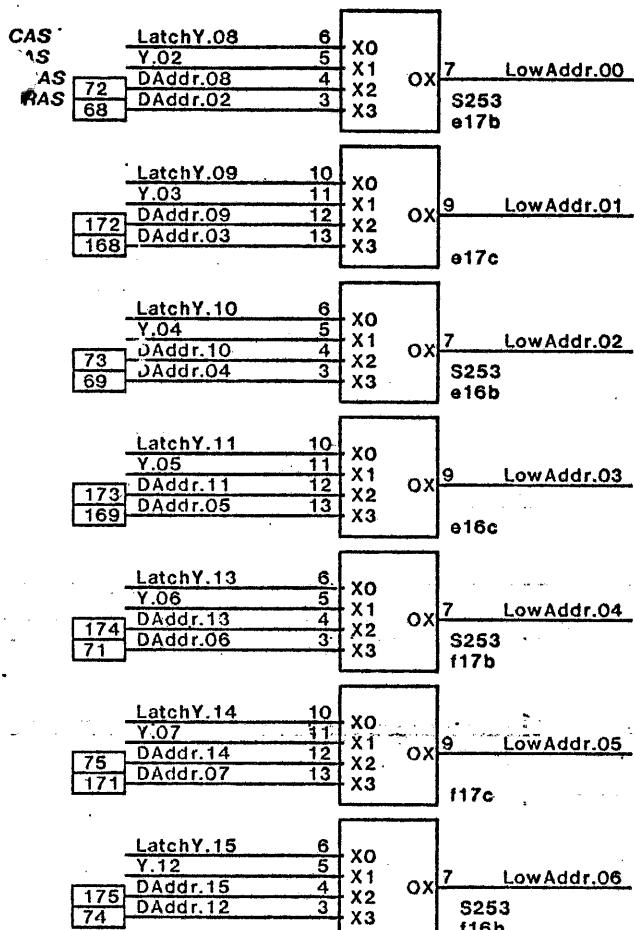
RFCL



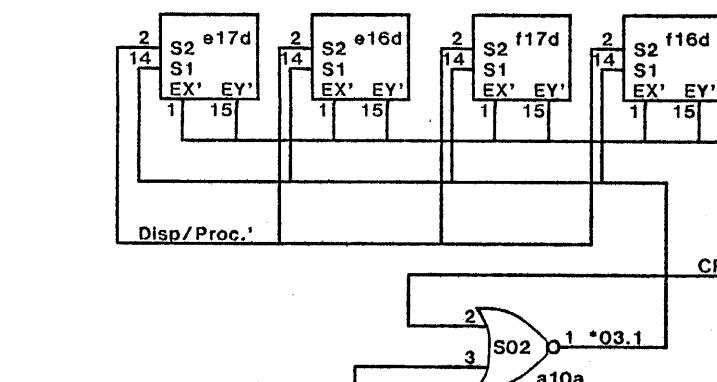
CRefresh'

Cycle2'

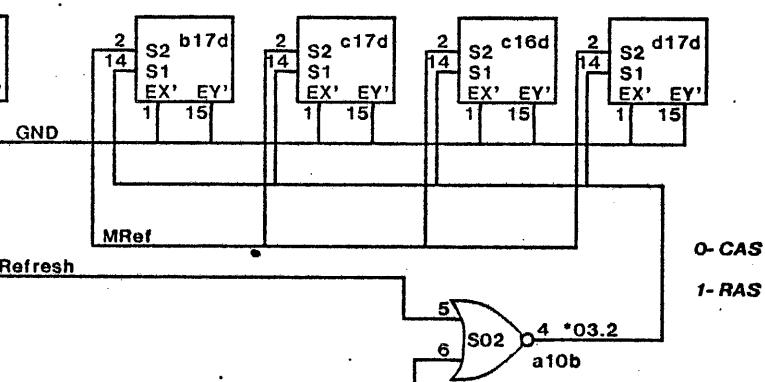




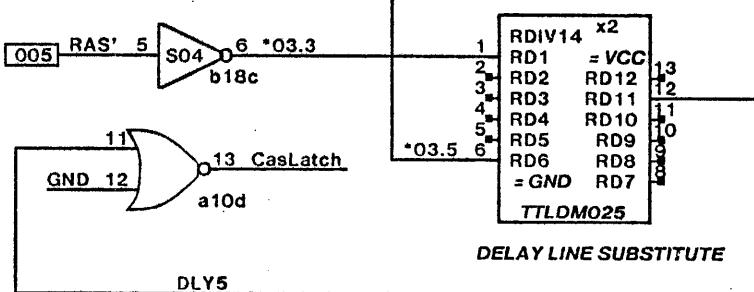
### *Low Bank Selection*



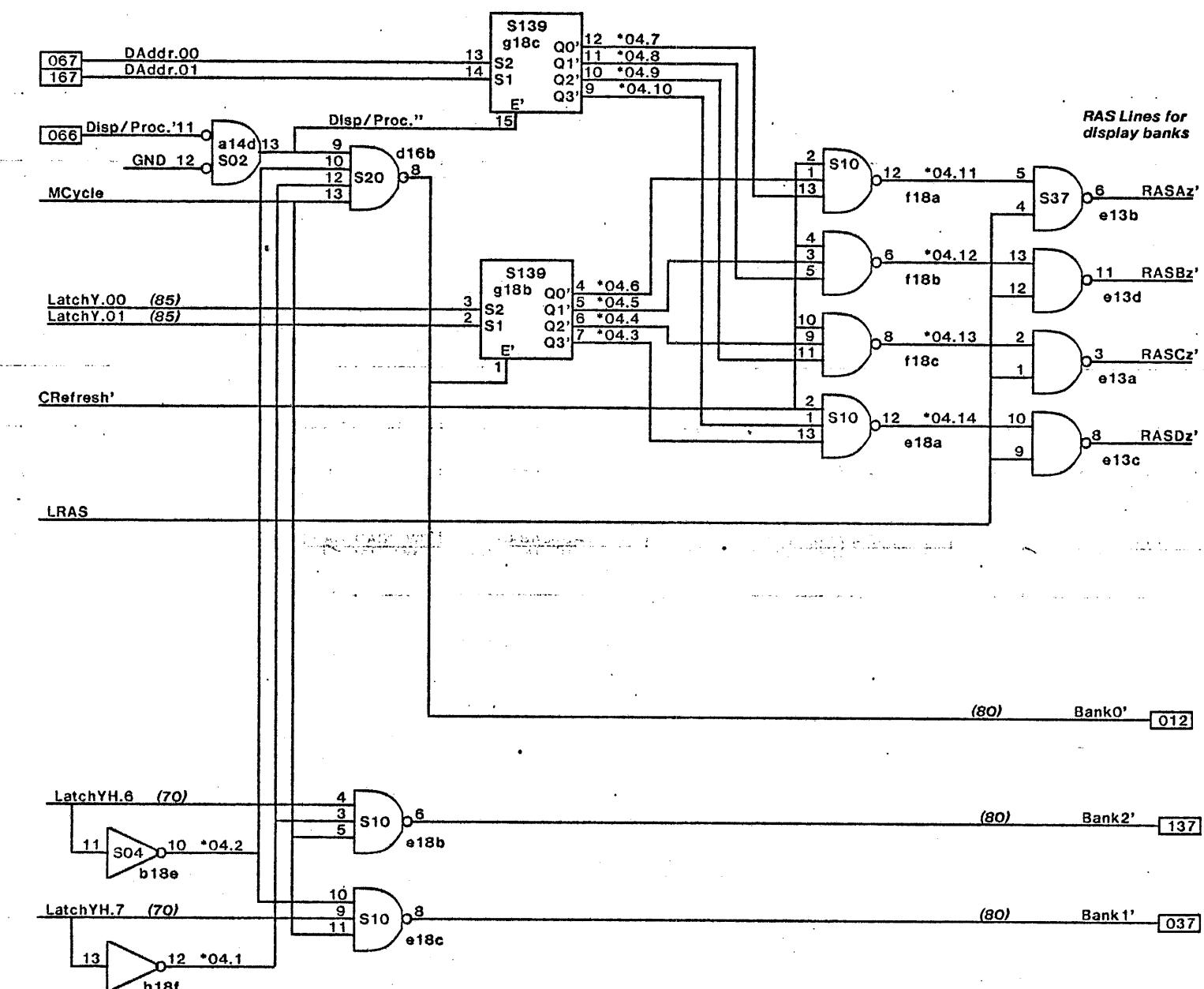
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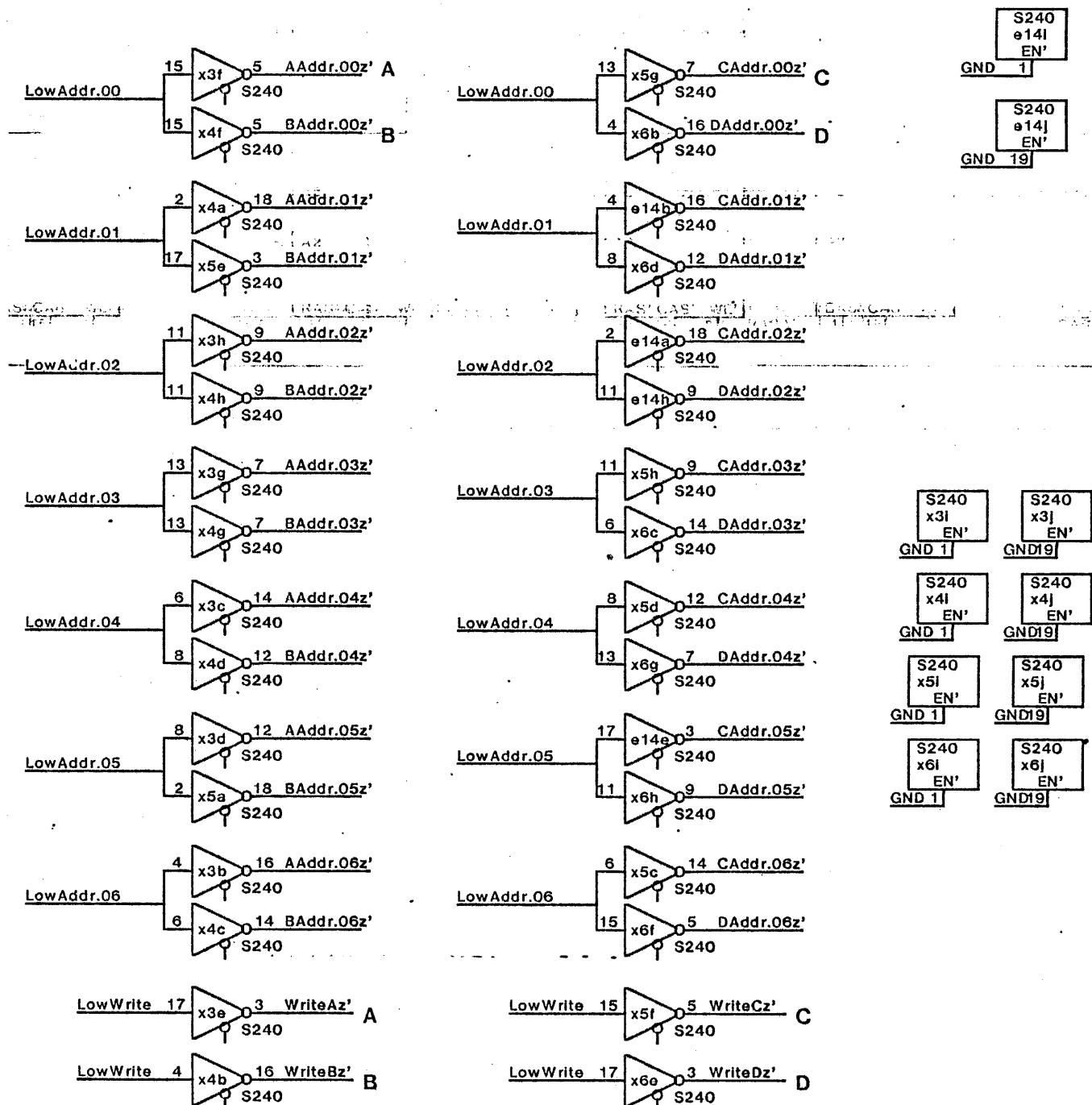
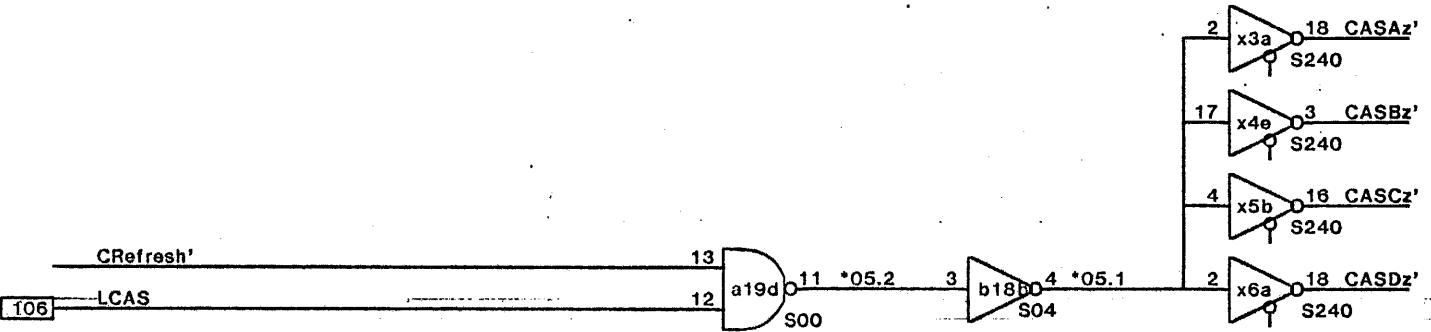


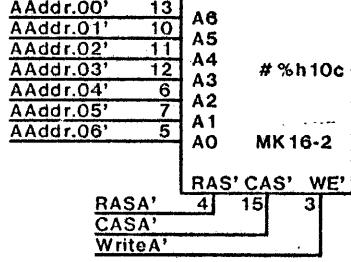
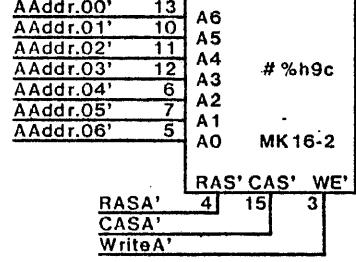
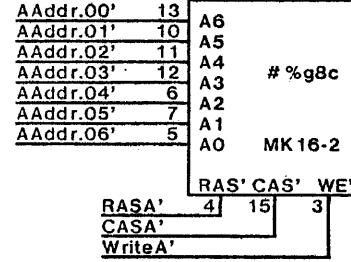
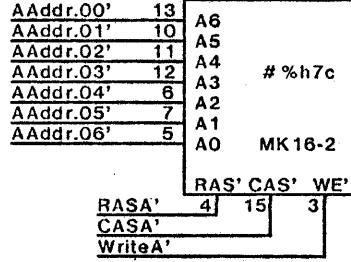
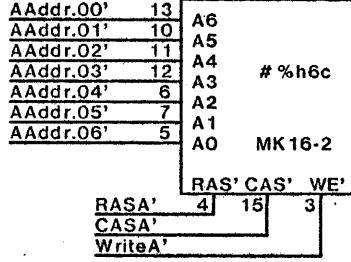
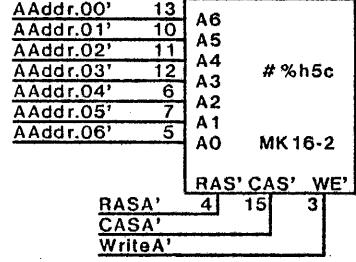
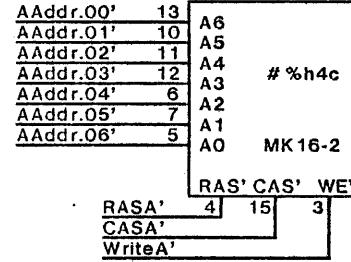
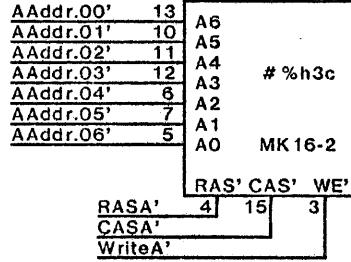
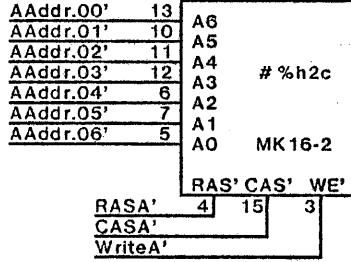
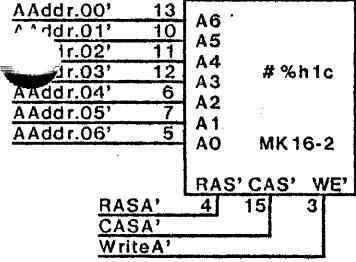
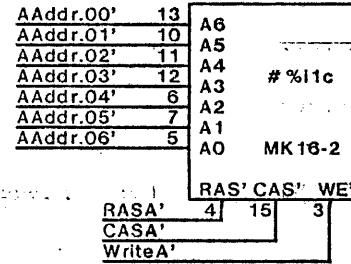
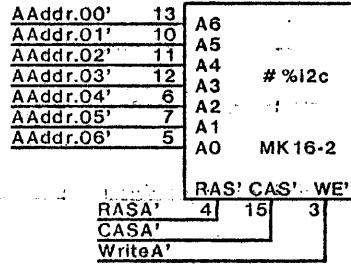
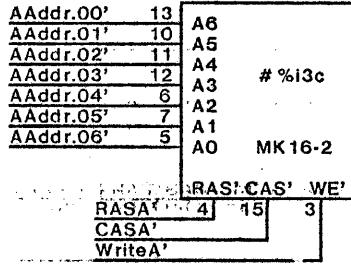
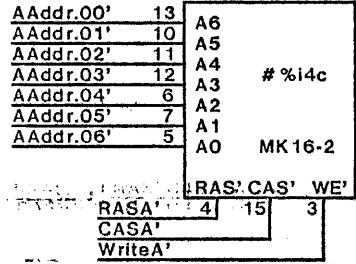
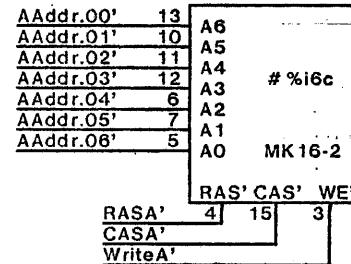
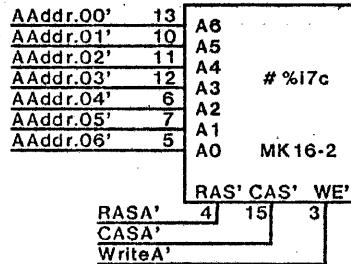
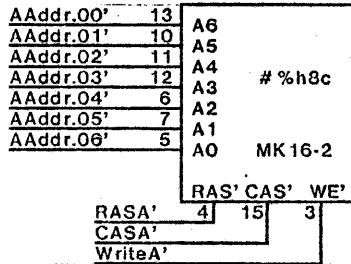
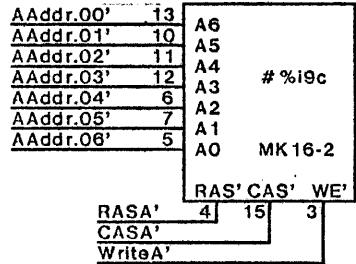
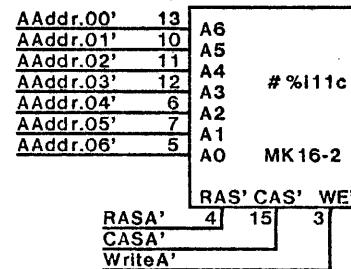
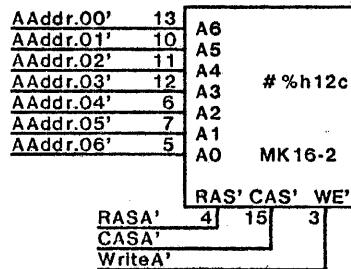
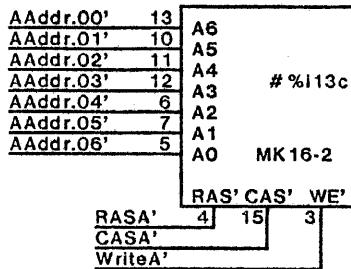
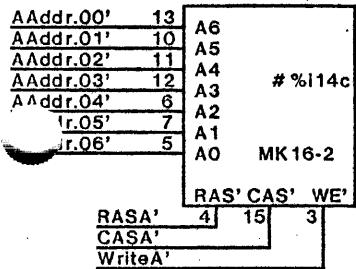
1	RDIV14	x1
2	RD1	= VCC
3	RD2	RD12
4	RD3	RD11
5	RD4	RD10
6	RD5	RD9
7	RD6	RD8
8	= GND	RD7
*03.4		
TTLDM025		

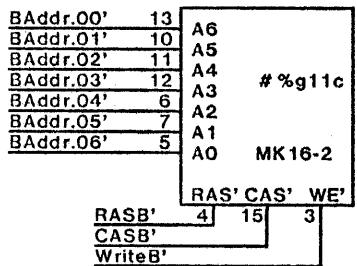
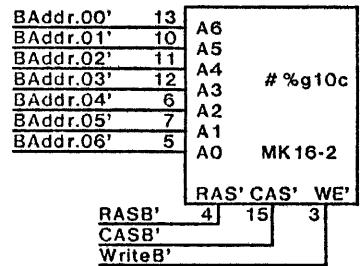
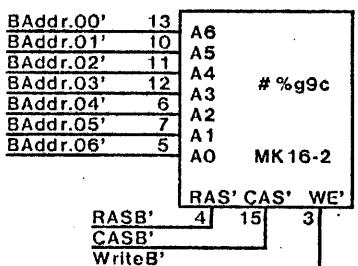
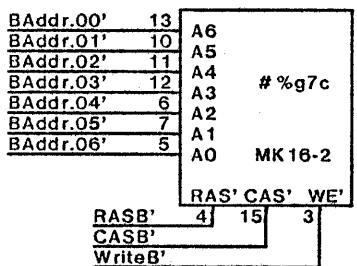
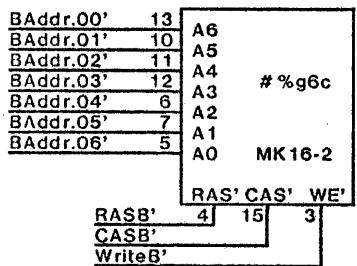
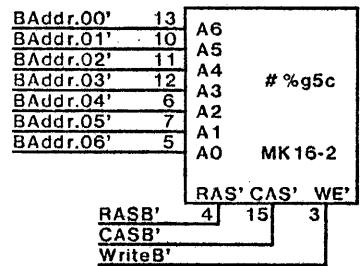
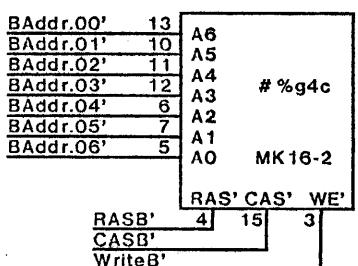
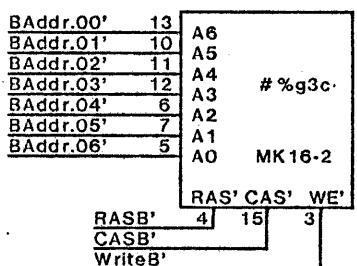
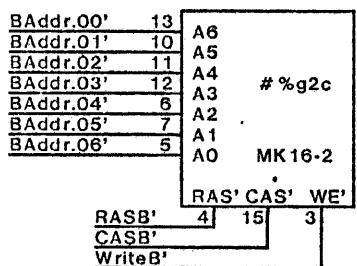
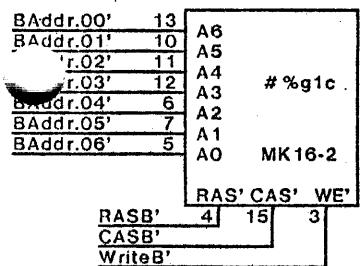
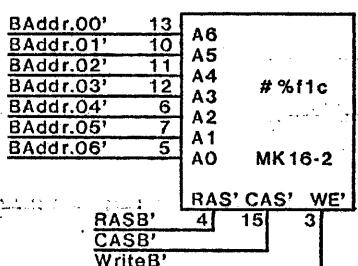
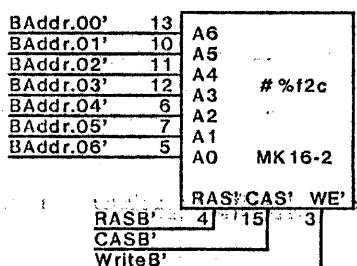
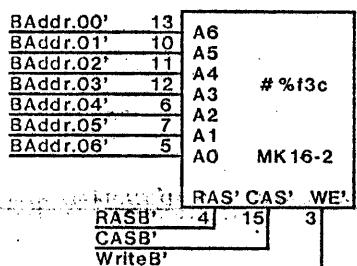
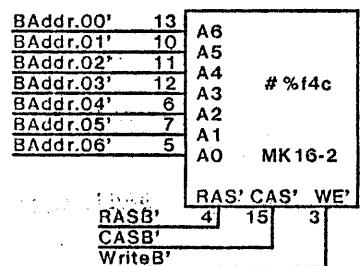
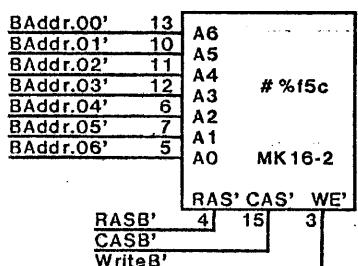
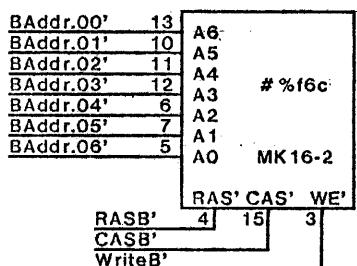
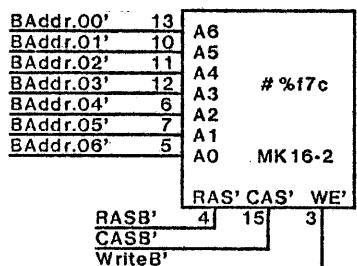
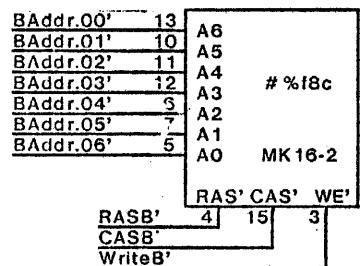
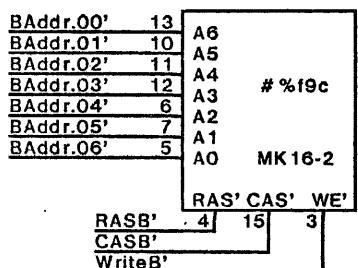
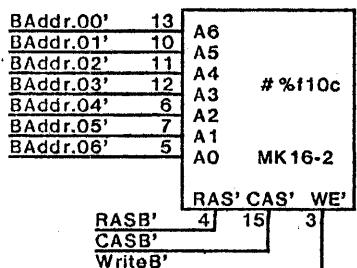
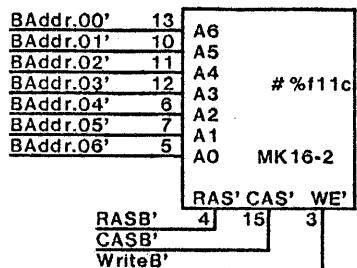
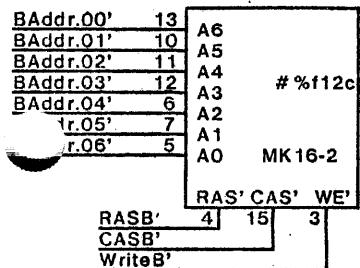


XEROX SDD	Project WS	Address Selection Logic RASDIy & LRASDIy	File EMCTL03.sil	Designer Crane	Rev D	Date 3/19/80	Page 3
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XEROX SDD	Project WS	Mem. Control/ Low Bank C	File EMCTL08.sil	Designer Crane/Cucinitti	Rev D	Date 2/14/80	Page 8
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DAddr.00'	13	A6
DAddr.01'	10	A5
DAddr.02'	11	A4
DAddr.03'	12	A3
'r.04'	6	A2
'r.05'	7	A1
'dr.06'	5	A0
		MK 16-2
RAS' CAS' WE'		
RASD'	4	15
CASD'		3
WrlteD'		

DAddr.00'	13	A6
DAddr.01'	10	A5
DAddr.02'	11	A4
DAddr.03'	12	A3
DAddr.04'	6	A2
DAddr.05'	7	A1
DAddr.06'	5	A0
		MK16-2
RAS' CAS' WE'		
RASD'	4	15
CASD'		3
WriteD'		

<u>DAddr.00'</u>	13	A6
<u>DAddr.01'</u>	10	A5
<u>DAddr.02'</u>	11	A4
<u>DAddr.03'</u>	12	A3
<u>DAddr.04'</u>	6	A2
<u>DAddr.05'</u>	7	A1
<u>DAddr.06'</u>	5	A0
		MK16-2
<u>RASD'</u>		RAS'
<u>CASD'</u>		CAS'
<u>WriteD'</u>		WE'
41	15	3

DAddr.00'	13	A6
DAddr.01'	10	A5
DAddr.02'	11	A4
DAddr.03'	12	A3
DAddr.04'	6	# %a11c
DAddr.05'	7	A2
DAddr.06'	5	A1
		A0 MK 16-2
<hr/>		
RAS'D' CAS'D' WE'		
RASD'	4	15
CASD'		3
WriteD'		

DAddr.00'	13	A6
DAddr.01'	10	A5
DAddr.02'	11	A4
DAddr.03'	12	A3 # %a9c
DAddr.04'	6	A2
DAddr.05'	7	A1
DAddr.06'	5	A0 MK 16-2
RAS' CAS' WE'		
RASD'	4	15
CASD'		3
WriteD'		

DAddr.00'	13	A6
DAddr.01'	10	A5
DAddr.02'	11	A4
DAddr.03'	12	A3 # %a8c
DAddr.04'	6	A2
DAddr.05'	7	A1
DAddr.06'	5	A0 MK16-2
		RAS' CAS' WE'
RASD'	4	15 3
CASD'		
WriteD'		

DAddr.00'	13	A6
DAddr.01'	10	A5
DAddr.02'	11	A4
DAddr.03'	12	A3
DAddr.04'	6	A2
DAddr.05'	7	A1
DAddr.06'	5	AO
		MK16-2
RAS'		RAS'
CAS'		CAS'
WriteD'		WE'

DAddr.00'	13	A6
DAddr.01'	10	A5
DAddr.02'	11	A4
DAddr.03'	12	A3 # %a6c
DAddr.04'	6	A2
DAddr.05'	7	A1
DAddr.06'	5	A0 MK 16-2
RAS' CAS' WE'		
RASD'	4	15
CASD'		3
WriteD'		

DAddr.00'	13	A6
DAddr.01'	10	A5
DAddr.02'	11	A4
DAddr.03'	12	A3
DAddr.04'	6	# %a4c
DAddr.05'	7	A2
DAddr.06'	5	A1
		A0
		MK 16-2
<hr/>		
RAS'D' CAS'D' WE'		
RASD'	4	15
CASD'		3
WriteD'		

DAddr.00'	13	A6
DAddr.01'	10	A5
DAddr.02'	11	A4
DAddr.03'	12	A3
DAddr.04'	6	# %a3c
DAddr.05'	7	A2
DAddr.06'	5	A1
		A0 MK16-2
		RAS' CAS' WE'
RASD'	4	15
CASD'		3
WriteD'		

DAddr.00'	13	A6
DAddr.01'	10	A5
DAddr.02'	11	A4
DAddr.03'	12	A3
DAddr.04'	6	A2
DAddr.05'	7	A1
DAddr.06'	5	AO
		MK16-2
RAS' CAS' WE'		
RASD'	41	15
CASD'		3
WriteD'		

DAddr.00'	13	A6
DAddr.01'	10	A5
DAddr.02'	11	A4
DAddr.03'	12	A3
DAddr.04'	6	# %a1c
DAddr.05'	7	A2
DAddr.06'	5	A1
		AO MK 16-2
RAS'		
RASD'	4	15
CAS'		
CASD'		3
WriteD'		

DAddr.00'	13	A6	
dr.01'	10	A5	
dr.02'	11	A4	# %b1c
dr.03'	12	A3	
DAddr.04'	6	A2	
DAddr.05'	7	A1	
DAddr.06'	5	AO	MK16-2
RAS' CAS' WE'			
RASD'	4	15	3
CASD'			
WriteD'			

DAddr.00'	13	A6
DAddr.01'	10	A5
DAddr.02'	11	A4
DAddr.03'	12	A3
DAddr.04'	6	# %b2c
DAddr.05'	7	A2
DAddr.06'	5	A1
		AO MK16-2
RAS' CAS' WE'		
RASD'	4	15
CASD'		3
WriteD'		

DAddr.00'	13	A6	
DAddr.01'	10	A5	
DAddr.02'	11	A4	# %b3c
DAddr.03'	12	A3	
DAddr.04'	6	A2	
DAddr.05'	7	A1	
DAddr.06'	5	AO	MK16-2
RAS' CAS' WE'			
RASD'	4	15	3
CASD'			
WriedD'			

DAddr.00'	13	A6	
DAddr.01'	10	A5	
DAddr.02'	11	A4	# %b4c
DAddr.03'	12	A3	
DAddr.04'	6	A2	
DAddr.05'	7	A1	
DAddr.06'	5	AO	MK 16-2
RAS' CAS' WE'			
RASD'	4	15	3
CASD'			
WriteD'			

DAddr.00'	13	A6	
DAddr.01'	10	A5	
DAddr.02'	11	A4	# %b5c
DAddr.03'	12	A3	
DAddr.04'	6	A2	
DAddr.05'	7	A1	
DAddr.06'	5	A0	MK 16-2
RAS' CAS' WE'			
RASD'	4	15	3
CASD'			
WriteD'			

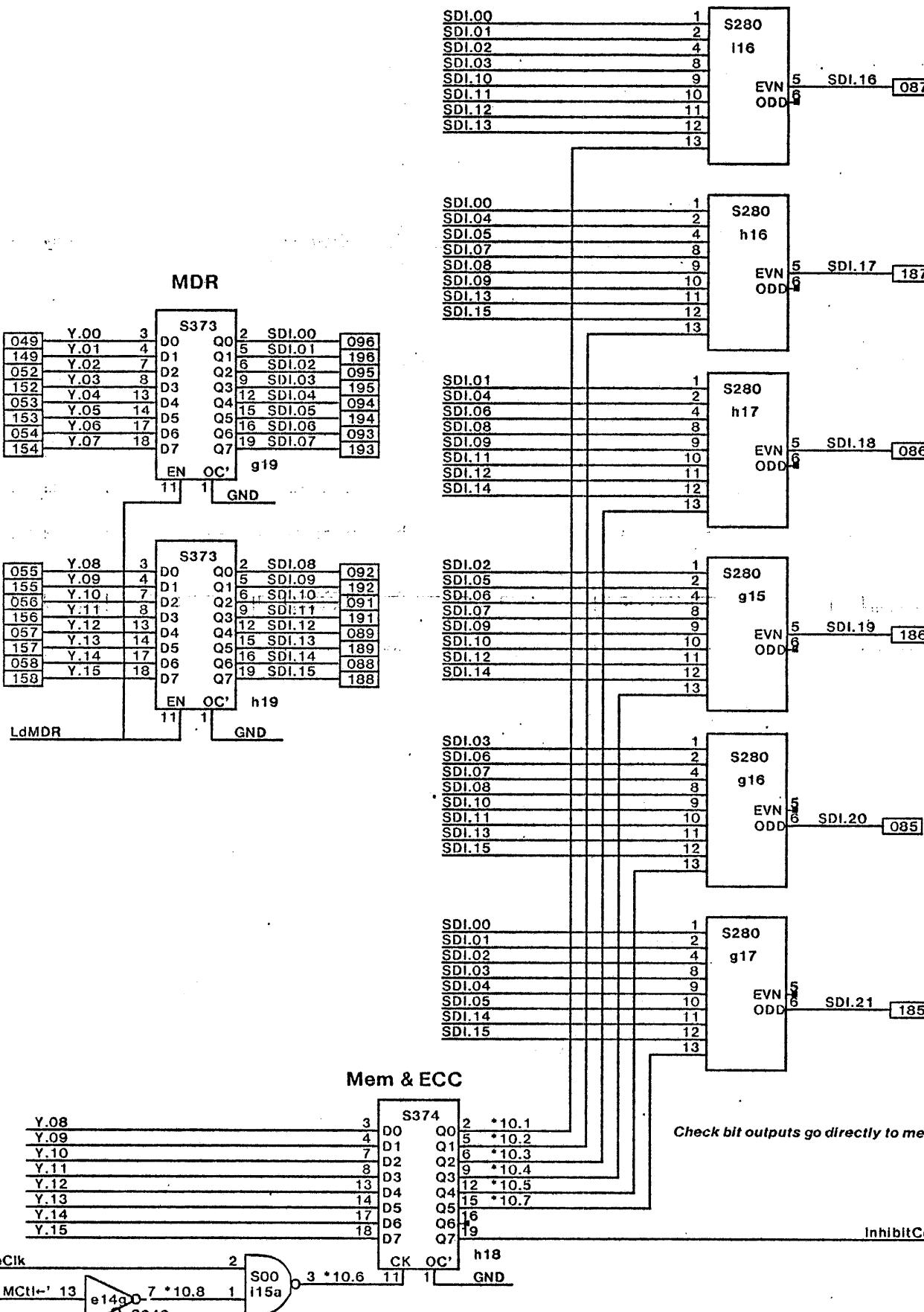
DAddr.00'	13	A6
DAddr.01'	10	A5
DAddr.02'	11	A4
DAddr.03'	12	A3
DAddr.04'	6	A2
DAddr.05'	7	A1
DAddr.06'	5	AO
		MK 16-2
RAS' CAS' WE'		
RASD'	4	15
CASD'		3
WriteD'		

DAddr.00'	13	A6	
DAddr.01'	10	A5	
DAddr.02'	11	A4	# %b7c
DAddr.03'	12	A3	
DAddr.04'	6	A2	
DAddr.05'	7	A1	
DAddr.06'	5	AO	MK16-2
		RAS' CAS' WE'	
RASD'	41	15	3
CASD'			
WriteD'			

DAddr.00'	13	A6	
DAddr.01'	10	A5	
DAddr.02'	11	A4	# %b9c
DAddr.03'	12	A3	
DAddr.04'	6	A2	
DAddr.05'	7	A1	
DAddr.06'	5	A0	MK 16-2
RAS' CAS' WE'			
RASD'	4	15	3
CASD'			
WriteD'			

DAddr.00'	13	A6	
DAddr.01'	10	A5	
DAddr.02'	11	A4	# %b10c
DAddr.03'	12	A3	
DAddr.04'	6	A2	-
DAddr.05'	7	A1	
DAddr.06'	5	A0	MK 16-2
RAS' CAS' WE'			
RASD'	4	15	3
CASD'			
WriteD'			

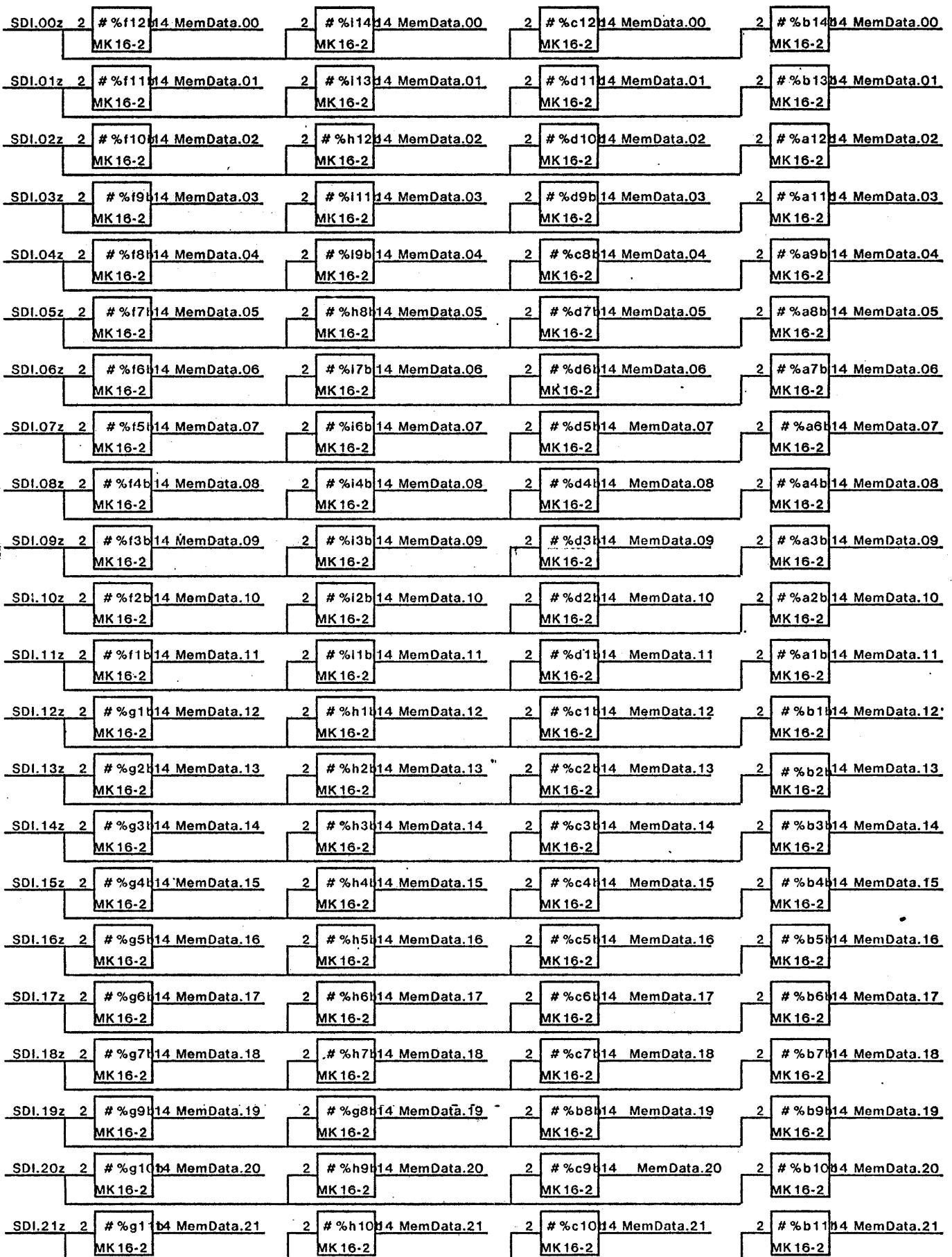
DAddr.00'	13	A6
DAddr.01'	10	A5
DAddr.02'	11	A4
DAddr.03'	12	A3
DAddr.04'	6	A2
DAddr.05'	7	A1
DAddr.06'	5	A0
		MK16-2
RAS' CAS' WE'		
RASD'	4	15
CASD'		3
WriteD'		



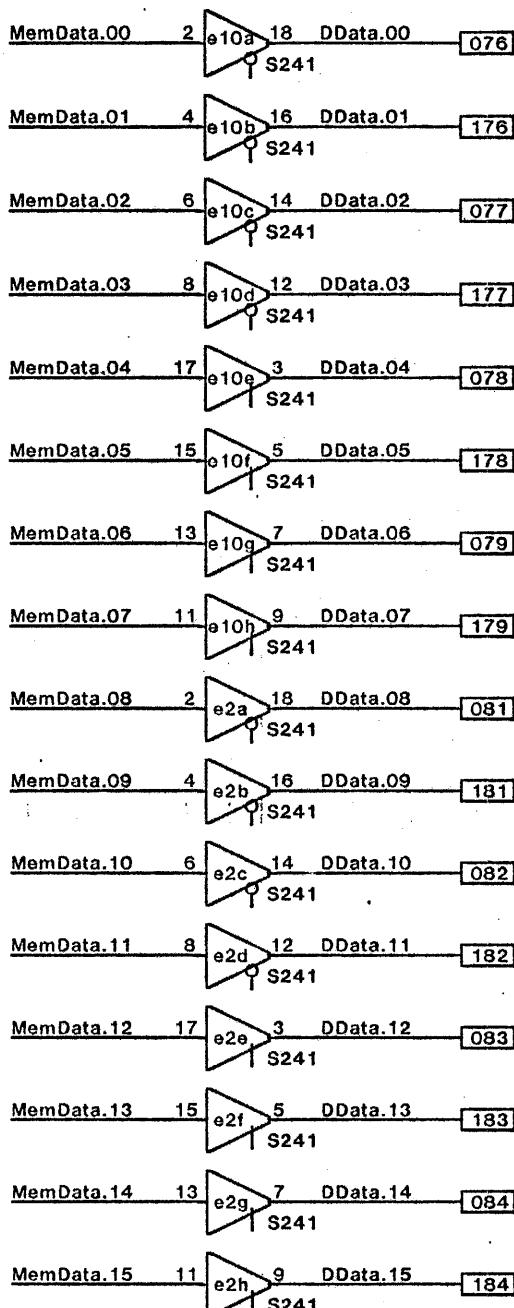
Normally, only correction enable is turned on. Other bits in Mem & ECC register are set to invert check bits for diagnostic purposes.

Data bits come from memory data register (MDR)

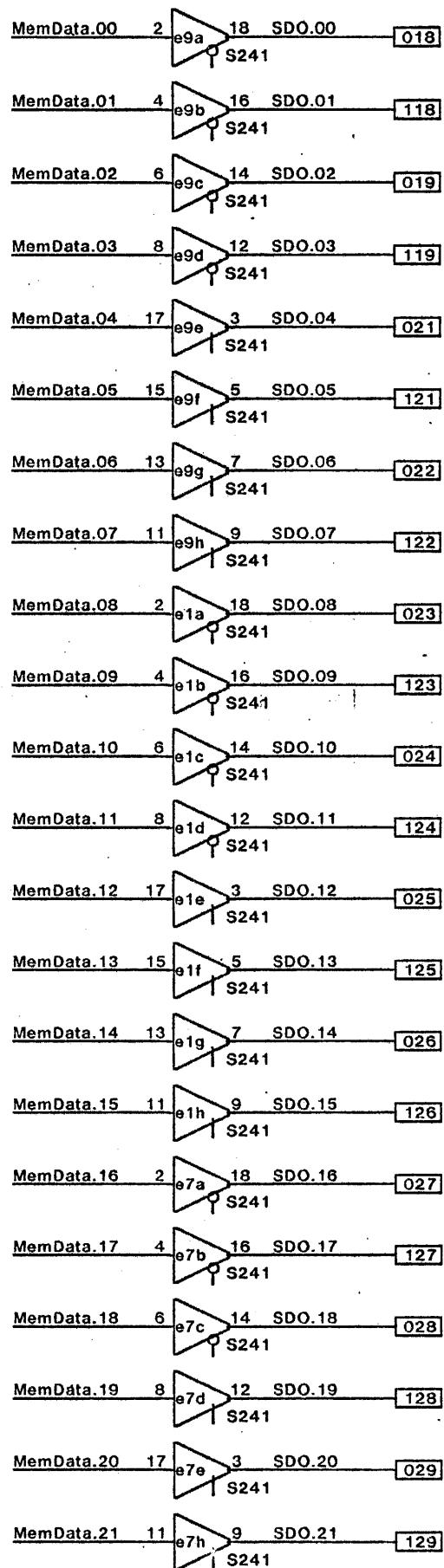
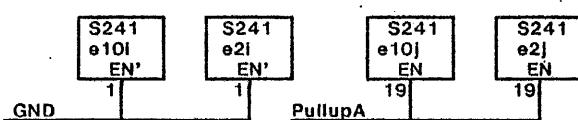
XEROX SDD	Project WS	Mem. Data Reg., Mem. Ctl. Reg. & Check Bit Generator	File EMCTL10.sil	Designer Crane	Rev D	Date 2/14/80	Page 10
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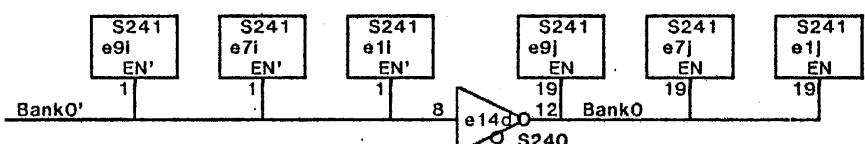
XEROX SDD	Project WS	Work Station Memory Bank0	File EMCTL11.sil	Designer Crane/Cucinitti	Rev D	Date 2/14/80	Page 11
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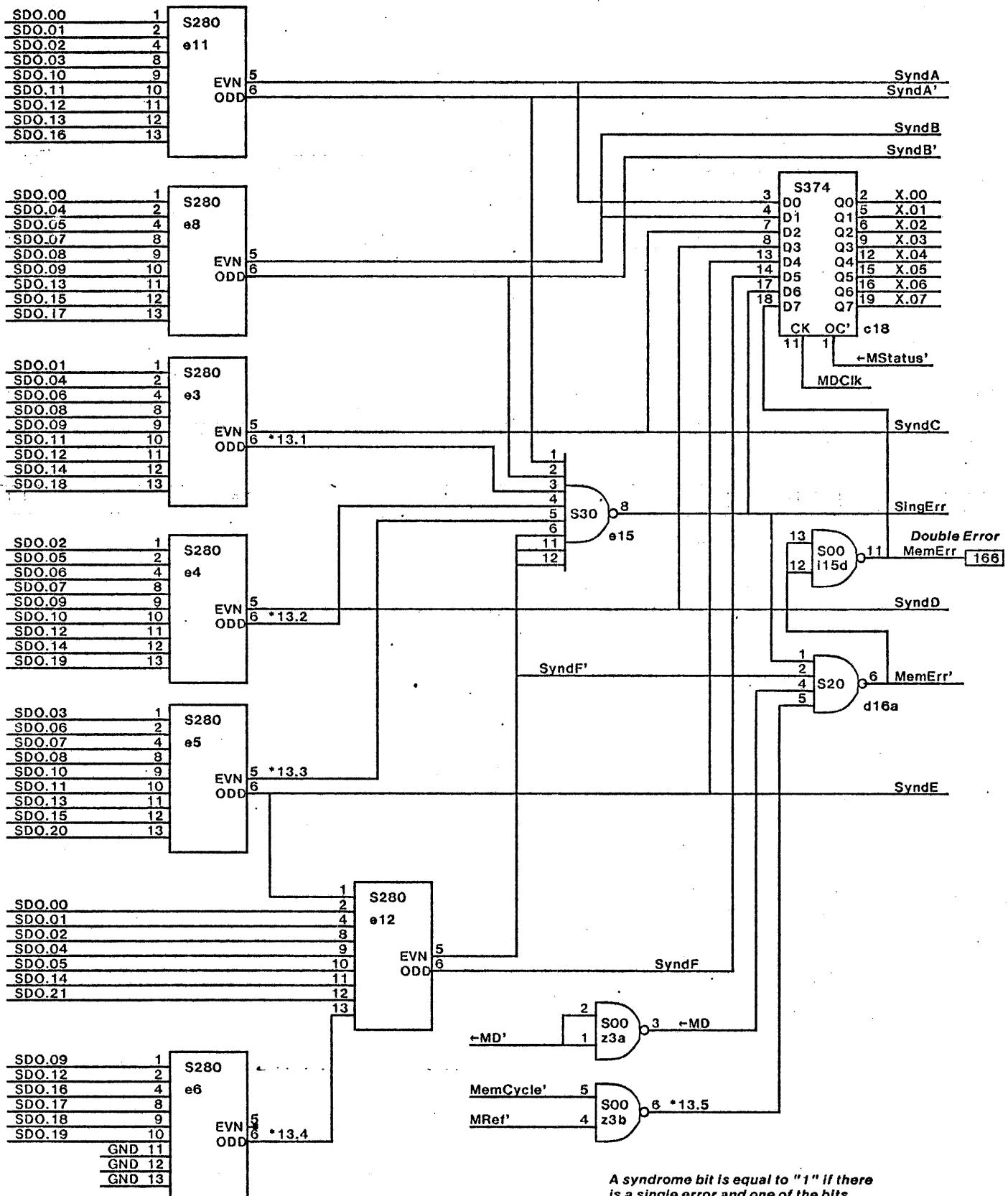
#### Display Data Buffers



#### Main Data Buffers

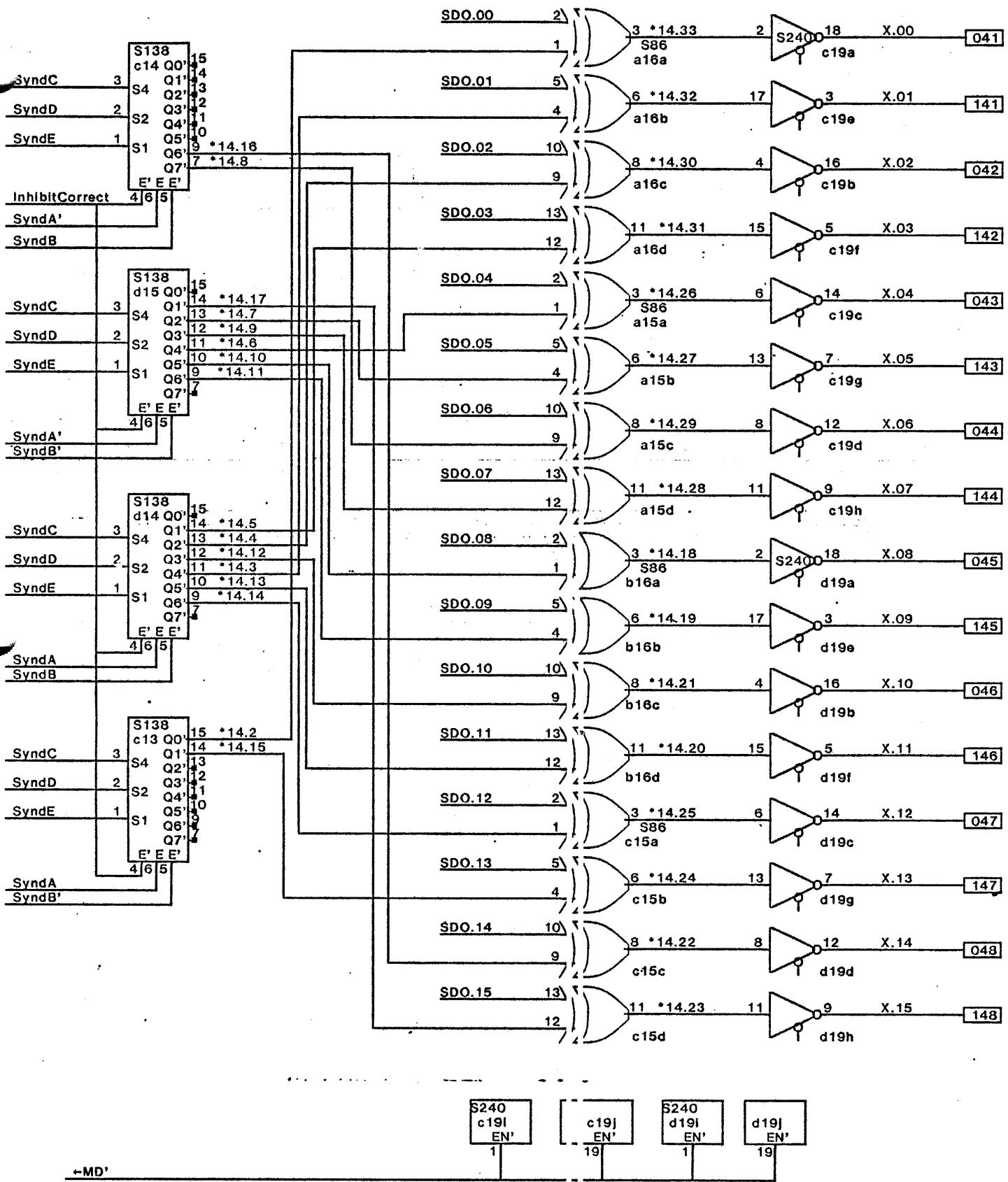


XEROX SDD	Project WS	Data Buffers Low Memory Bank	File EMCTL12.sil	Designer Crane/Cucinitti	Rev D	Date 3/19/80	Page 12
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A syndrome bit is equal to "1" if there is a single error and one of the bits it covers is in error.  
Syndrome bits A-E point to the bad bit.

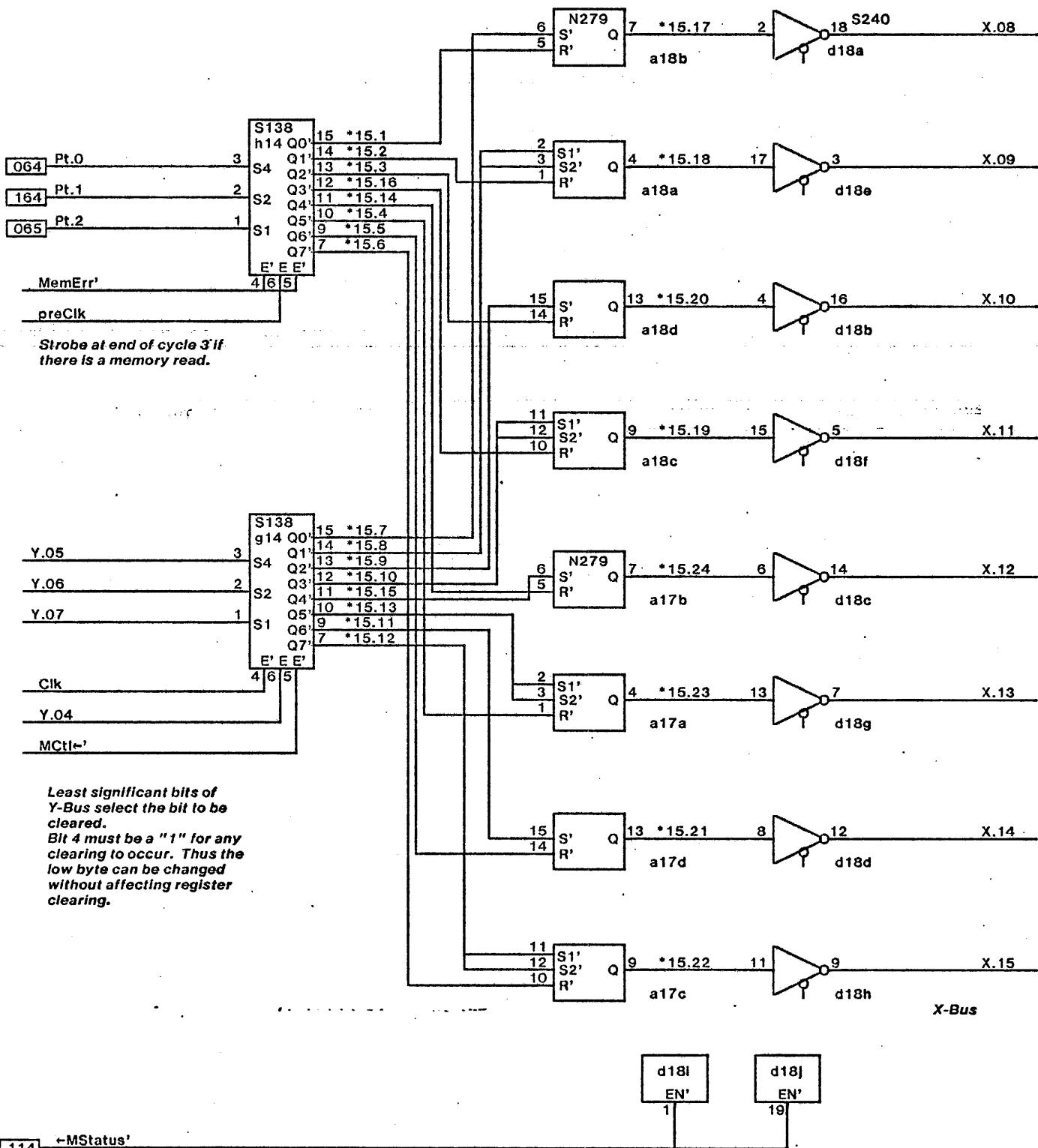
XEROX SDD	Project WS	Syndrome Generator	File EMCTL13.sil	Designer Crane	Rev D	Date 2/14/80	Page 13
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Syndrome Bits point to the bad bit. SyndA is most significant bit & SyndE is LSB.  
Syndrome bit is a '1' if one of the bits it covers is in error.

## Errors Register

Bit is 1 if there was an error.

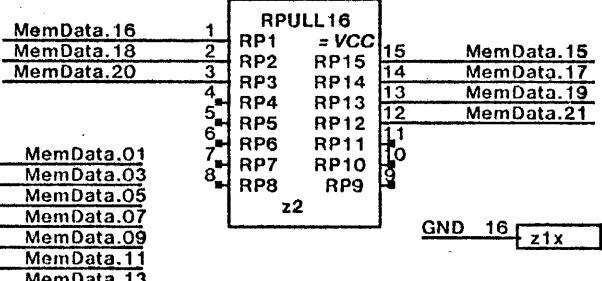


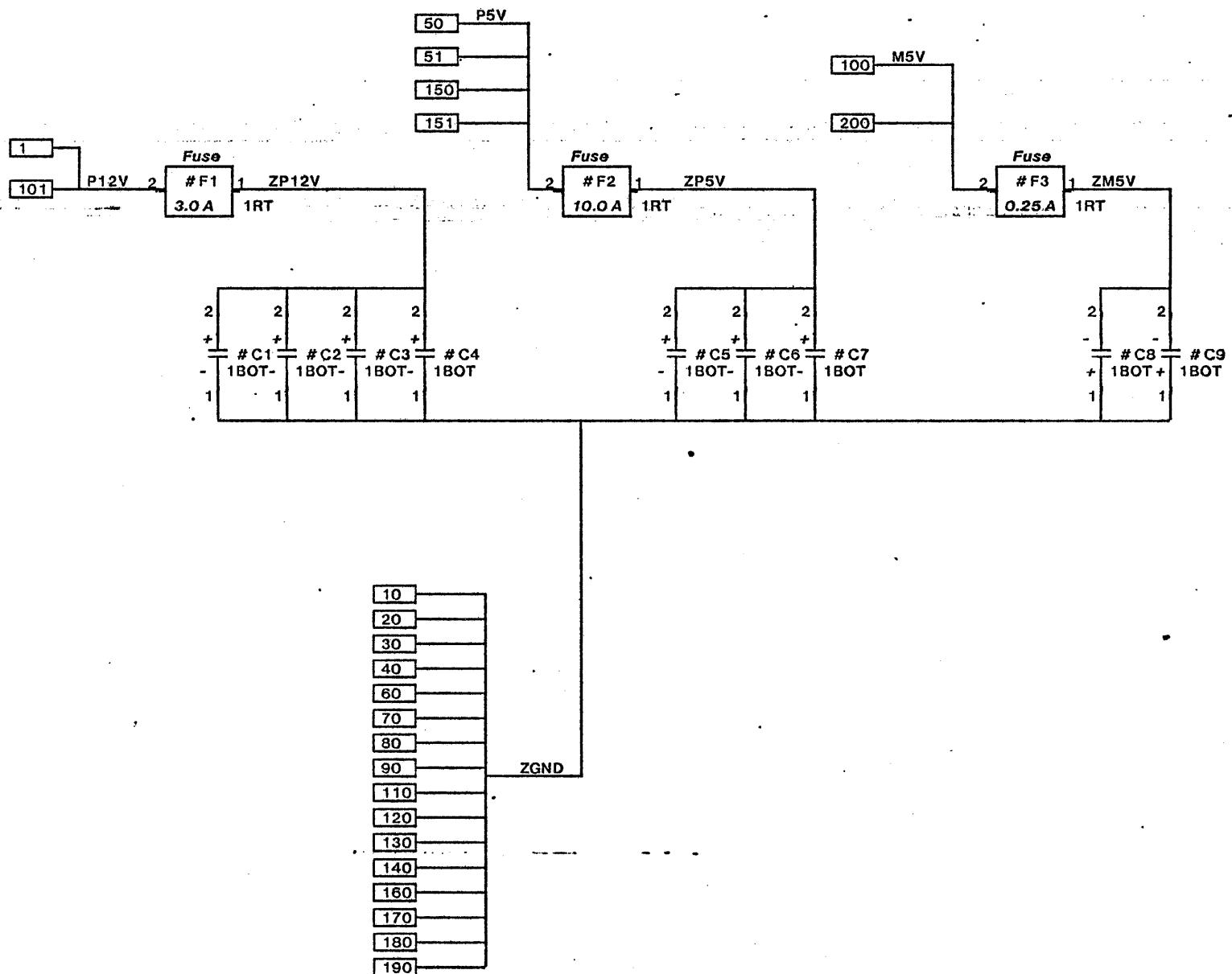
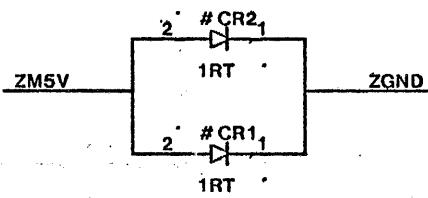
114  $\rightarrow$  MStatus'

SDI.00	2' #R1 1	SDI.00z
	1RT	
SDI.01	2' #R2 1	SDI.01z
	1RT	
SDI.02	2' #R3 1	SDI.02z
	1RT	
SDI.03	2' #R4 1	SDI.03z
	1RT	
SDI.04	2' #R5 1	SDI.04z
	1RT	
SDI.05	2' #R6 1	SDI.05z
	1RT	
SDI.06	2' #R7 1	SDI.06z
	1RT	
SDI.07	2' #R8 1	SDI.07z
	1RT	
SDI.08	2' #R9 1	SDI.08z
	1RT	
SDI.09	2' #R10 1	SDI.09z
	1RT	
SDI.10	2' #R11 1	SDI.10z
	1RT	
SDI.11	2' #R12 1	SDI.11z
	1RT	
SDI.12	2' #R13 1	SDI.12z
	1RT	
SDI.13	2' #R14 1	SDI.13z
	1RT	
SDI.14	2' #R15 1	SDI.14z
	1RT	
SDI.15	2' #R16 1	SDI.15z
	1RT	
SDI.16	2' #R17 1	SDI.16z
	1RT	
SDI.17	2' #R18 1	SDI.17z
	1RT	
SDI.18	2' #R19 1	SDI.18z
	1RT	
SDI.19	2' #R20 1	SDI.19z
	1RT	
SDI.20	2' #R21 1	SDI.20z
	1RT	
SDI.21	2' #R22 1	SDI.21z
	1RT	
PullupA	2' #R23 1	ZP5V
	1RT	
PullupB	2' #R64 1	ZP5V
	1RT	
RFCL	2' #R65 1	ZP5V
	1RT	

CASA'	2' #R24 1	CASAz'	CASC'	2' #R44 1	CASCz'
	1RT			1RT	
WriteA'	2' #R25 1	WriteAz'	WriteC'	2' #R45 1	WriteCz'
	1RT			1RT	
AAddr.00'	2' #R26 1	AAddr.00z'	CAddr.00'	2' #R46 1	CAddr.00z'
	1RT			1RT	
RASA'	2' #R27 1	RASAz'	RASC'	2' #R47 1	RASCz'
	1RT			1RT	
AAddr.03'	2' #R28 1	AAddr.03z'	CAddr.03'	2' #R48 1	CAddr.03z'
	1RT			1RT	
AAddr.06'	2' #R29 1	AAddr.06z'	CAddr.06'	2' #R49 1	CAddr.06z'
	1RT			1RT	
AAddr.02'	2' #R30 1	AAddr.02z'	CAddr.02'	2' #R50 1	CAddr.02z'
	1RT			1RT	
AAddr.04'	2' #R31 1	AAddr.04z'	CAddr.04'	2' #R51 1	CAddr.04z'
	1RT			1RT	
AAddr.01'	2' #R32 1	AAddr.01z'	CAddr.01'	2' #R52 1	CAddr.01z'
	1RT			1RT	
AAddr.05'	2' #R33 1	AAddr.05z'	CAddr.05'	2' #R53 1	CAddr.05z'
	1RT			1RT	
CASB'	2' #R34 1	CASBz'	CASD'	2' #R54 1	CASDz'
	1RT			1RT	
WriteB'	2' #R35 1	WriteBz'	WriteD'	2' #R55 1	WriteDz'
	1RT			1RT	
BAddr.00'	2' #R36 1	BAddr.00z'	DAddr.00'	2' #R56 1	DAddr.00z'
	1RT			1RT	
RASB'	2' #R37 1	RASBz'	RASD'	2' #R57 1	RASDz'
	1RT			1RT	
BAddr.03'	2' #R38 1	BAddr.03z'	DAddr.03'	2' #R58 1	DAddr.03z'
	1RT			1RT	
BAddr.06'	2' #R39 1	BAddr.06z'	DAddr.06'	2' #R59 1	DAddr.06z'
	1RT			1RT	
BAddr.02'	2' #R40 1	BAddr.02z'	DAddr.02'	2' #R60 1	DAddr.02z'
	1RT			1RT	
BAddr.04'	2' #R41 1	BAddr.04z'	DAddr.04'	2' #R61 1	DAddr.04z'
	1RT			1RT	
BAddr.01'	2' #R42 1	BAddr.01z'	DAddr.01'	2' #R62 1	DAddr.01z'
	1RT			1RT	
BAddr.05'	2' #R43 1	BAddr.05z'	DAddr.05'	2' #R63 1	DAddr.05z'
	1RT			1RT	

MemData.00	1	RPULL16	1	RP1 = VCC
MemData.02	2	RP2	2	RP15
MemData.04	3	RP3	3	RP14
MemData.06	4	RP4	4	RP13
MemData.08	5	RP5	5	RP12
MemData.10	6	RP6	6	RP11
MemData.12	7	RP7	7	RP10
MemData.14	8	RP8	8	RP9
		z1		z2





CASA' 1 (C) tl #TP001  
WriteA' 1 (C) tl #TP002  
AAddr.00' 1 (C) tl #TP003  
RASA' 1 (C) tl #TP004  
AAddr.03' 1 (C) tl #TP005  
AAddr.06' 1 (C) tl #TP006  
AAddr.02' 1 (C) tl #TP007  
AAddr.04' 1 (C) tl #TP008  
AAddr.01' 1 (C) tl #TP009  
AAddr.05' 1 (C) tl #TP010

CASB' 1 (C) tl #TP011  
WriteB' 1 (C) tl #TP012  
BAddr.00' 1 (C) tl #TP013  
RASB' 1 (C) tl #TP014  
BAddr.03' 1 (C) tl #TP015  
BAddr.06' 1 (C) tl #TP016  
BAddr.02' 1 (C) tl #TP017  
BAddr.04' 1 (C) tl #TP018  
BAddr.01' 1 (C) tl #TP019  
BAddr.05' 1 (C) tl #TP020

CASC' 1 (C) tl #TP021  
WriteC' 1 (C) tl #TP022  
CAddr.00' 1 (C) tl #TP023  
RASC' 1 (C) tl #TP024  
CAddr.03' 1 (C) tl #TP025  
CAddr.06' 1 (C) tl #TP026  
CAddr.02' 1 (C) tl #TP027  
CAddr.04' 1 (C) tl #TP028  
CAddr.01' 1 (C) tl #TP029  
CAddr.05' 1 (C) tl #TP030

CASD' 1 (C) tl #TP031  
WriteD' 1 (C) tl #TP032  
DAddr.00' 1 (C) tl #TP033  
RASD' 1 (C) tl #TP034  
DAddr.03' 1 (C) tl #TP035  
DAddr.06' 1 (C) tl #TP036  
DAddr.02' 1 (C) tl #TP037  
DAddr.04' 1 (C) tl #TP038  
DAddr.01' 1 (C) tl #TP039  
DAddr.05' 1 (C) tl #TP040

SDI.00z 1 (C) tl #TP041  
SDI.01z 1 (C) tl #TP042  
SDI.02z 1 (C) tl #TP043  
SDI.03z 1 (C) tl #TP044  
SDI.04z 1 (C) tl #TP045  
SDI.05z 1 (C) tl #TP046  
SDI.06z 1 (C) tl #TP047  
SDI.07z 1 (C) tl #TP048  
SDI.08z 1 (C) tl #TP049  
SDI.09z 1 (C) tl #TP050  
SDI.10z 1 (C) tl #TP051  
SDI.11z 1 (C) tl #TP052  
SDI.12z 1 (C) tl #TP053  
SDI.13z 1 (C) tl #TP054  
SDI.14z 1 (C) tl #TP055  
SDI.15z 1 (C) tl #TP056  
SDI.16z 1 (C) tl #TP057  
SDI.17z 1 (C) tl #TP058  
SDI.18z 1 (C) tl #TP059  
SDI.19z 1 (C) tl #TP060  
SDI.20z 1 (C) tl #TP061  
SDI.21z 1 (C) tl #TP062

MCycle 1 (C) tl #TP085

LatchY.02 1 (C) tl #TP086  
LatchY.03 1 (C) tl #TP087  
LatchY.05 1 (C) tl #TP088  
LatchY.06 1 (C) tl #TP089  
LatchY.07 1 (C) tl #TP090  
LatchY.08 1 (C) tl #TP091  
LatchY.09 1 (C) tl #TP092  
LatchY.10 1 (C) tl #TP093  
LatchY.11 1 (C) tl #TP094  
LatchY.13 1 (C) tl #TP095  
LatchY.14 1 (C) tl #TP096  
LatchY.15 1 (C) tl #TP097

MemData.00 1 (C) tl #TP063  
MemData.01 1 (C) tl #TP064  
MemData.02 1 (C) tl #TP065  
MemData.03 1 (C) tl #TP066  
MemData.04 1 (C) tl #TP067  
MemData.05 1 (C) tl #TP068  
MemData.06 1 (C) tl #TP069  
MemData.07 1 (C) tl #TP070  
MemData.08 1 (C) tl #TP071  
MemData.09 1 (C) tl #TP072  
MemData.10 1 (C) tl #TP073  
MemData.11 1 (C) tl #TP074  
MemData.12 1 (C) tl #TP075  
MemData.13 1 (C) tl #TP076  
MemData.14 1 (C) tl #TP077  
MemData.15 1 (C) tl #TP078  
MemData.16 1 (C) tl #TP079  
MemData.17 1 (C) tl #TP080  
MemData.18 1 (C) tl #TP081  
MemData.19 1 (C) tl #TP082  
MemData.20 1 (C) tl #TP083  
MemData.21 1 (C) tl #TP084

RFCL 1 (C) tl #TP098

PullupB 1 (C) tl #TP099

XEROX SDD	Project WS	TEST	POINTS	File EMCTL18.sil	Designer Crane/Cucinitti	Rev D	Date 3/19/80	Page 18
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ITEM	DESCRIPTION	DWG #	QTY	REMARKS
1	INTEGRATED CIRCUIT SN74S00	733w00318	3	
2	INTEGRATED CIRCUIT SN74S02	733w01643	3	
3	INTEGRATED CIRCUIT SN74S04	733w00319	1	
4	INTEGRATED CIRCUIT SN74S10	733w01606	3	
5	INTEGRATED CIRCUIT SN74S20	733w01619	1	
6	INTEGRATED CIRCUIT SN74S30	733w01645	1	
7	INTEGRATED CIRCUIT SN74S37	733w02136	1	
8	INTEGRATED CIRCUIT SN74S74	733w01771	2	
9	INTEGRATED CIRCUIT SN74S86	733w01648	4	
10	INTEGRATED CIRCUIT SN74S138	733w01616	6	
11	INTEGRATED CIRCUIT SN74S139	733w01669	1	
12	INTEGRATED CIRCUIT SN74S240	733w01633	9	
13	INTEGRATED CIRCUIT SN74S241	733w01634	5	
14	INTEGRATED CIRCUIT SN74S253	733w01636	8	
15	INTEGRATED CIRCUIT SN74279	733w00341	2	
16	INTEGRATED CIRCUIT SN74S280	733w01638	13	
17	INTEGRATED CIRCUIT SN74S373	733w01699	4	
18	INTEGRATED CIRCUIT SN74S374	733w01640	2	
19	INTEGRATED CIRCUIT SN74LS393	733w01663	1	
20	MEMORY CHIP 16K MK4116-2	733w01512	88	
21	CAPACITOR 0.1uf 50v	102P20600	115	
22	CAPACITOR 20uf 15v	702W07301	5	C5 --> C9 (alt. 25uf 12v 702W05601)
23	CAPACITOR 10uf 25v	702W08901	4	C1 --> C4
24	DELAY LINE 25 ns Eng Components Co.	744W00001	2	X1 + X2 TTLDM025
25	DIODE 1N5820	107P10105	2	CR1 + CR2
26	FUSE 0.25 A	708W10302	1	F3
27	FUSE 3.0 A	708W11002	1	F1
28	FUSE 10.0 A	708W11402	1	F2
29	R-DIP 1.0 k ohm	703W13291	2	Z1 + Z2
30	RESISTOR 18 ohm 1/4 watt 5 %	703W28088	12	R24,R25,R27,R34,R35,R37,R44,R45, R47,R54,R55 + R57
31	RESISTOR 20 ohm 1/4 watt 5 %	703W28188	28	R26,R28 --> R33,R36,R38 --> R43, R46,R48 --> R53,R56,R58 --> R63
32	RESISTOR 27 ohm 1/4 watt 5 %	703W28488	22	R1 --> R22
33	RESISTOR 1.0 k ohm 1/4 watt 5 %	703W32288	3	R23,R64 + R65
34	PWB	140P11229	1	
35	BOARD EXTRACTOR	003P80513	2	
36	STIFFENER (front)	596P54167	1	
37	STIFFENER (back)	030P83244	1	
38	RIVETS	320W13201	7	

XEROX SDD	Project WS	MATERIAL LIST Reference Memory Control Module	File EMCTL19.sil	Designer Crane	Rev D	Date 3/19/80	Page 19
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## Error Correction Logic

### Code Table

The codes have been optimized for use with 9 input parity chips (S280). Each row represents the inputs to a single chip. 8 inputs are used when writing and 9 are used when reading.

(Check bit F is parity over entire word. X's are omitted from the group of bits whose overall parity remains fixed.)

	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	a	b	c	d	e	f
a	x	x	x	x							x	x	x	x			x					
b	x				x	x		x	x	x					x		x					
c		x			x		x		x	x		x	x		x			x				
d			x			x	x	x		x	x	x		x					x			
e				x			x	x	x		x	x		x		x					x	
f	x	x	x	x	x	x										x	x				x	

Parity over all 22 bits

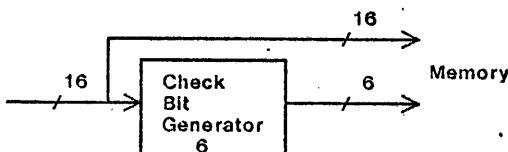
Data Bits

Check Bits

### Writing

Check bits written into memory are parity calculated over the data bits in the corresponding row.

Check bits a-d are odd parity and bits e-f are even parity. Bit f is really parity over the whole word, but the number of bits directly used to generate bit F is only 8 since the other data bits are cancelled out by other check bits.

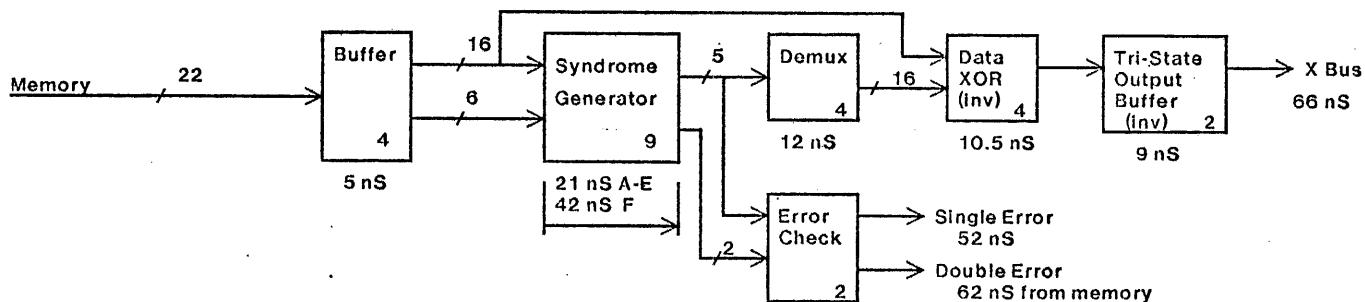


Parity checker chips  
Delay =  $1.15(21) = 24 \text{ nS}$

### Reading

All bits from rows A-E are used for the corresponding syndrome bit. (Stored parity: A-D = odd, E,F = even)

All 22 bits of the stored memory word are included in generation of syndrome bit F.



Numbers inside boxes are the number of chips used for the function.

Numbers below boxes are maximum delays from TI TTL Data book.  
15% is added below to allow for board propagation time

Total Delay for Data =  $1.15(57.5) = 66 \text{ nS}$  or 61 nS without buffer

### Error Check Possibilities

Syndrome	Meaning
OR A-F	Synd F
0	No error or >2 errors
0	Not Possible
1	Dbl error detected
1	Single error corrected

## Map References

The memory system supports a 22 bit virtual address space divided into pages of 256 words each. Thus, 14 bits specify the page number and 8 bits specify the location within the page.

The physical memory system will support up to 256K of real memory, i.e. an 18 bit address space. Thus there is a 10 bit physical page number and 8 bits as above for specifying the location within the page.

Since the virtual space is larger than the physical space, a mapping is performed between the 14 bit virtual page number and the 10 bit physical page number. The 14 bit virtual page number is used to access one of 16K locations which comprise the map in main memory. The accessed memory location (map entry) contains the 10 bit physical page number and status bits for the page (write protect, referenced, dirty).

Map References to the memory system are done by specifying MapRef in the microcode and sending the 22 bit virtual memory address to the memory via the Y (16 bits) and YH (6 bits) busses.

This causes an access into the map, a 16K word segment of main memory located between 65K and 80K. Specifying MapRef forces access to the 65K-80K bank while the high 14 bits of the 22 bit virtual address are used to access a word within that 16K bank.

